GHENT UNIVERSITY

Course Specifications

Valid as from the academic year 2020-2021

Embedded Systems: Hardware Synthesis (E731037)

Due to Covid 19, the education and evaluation methods may vary from the information displayed in the schedules and course details. Any changes will be communicated on Ufora.

Course size *(nominal values; actual values may depend on programme)*

Credits 6.0 **Study time 180 h** **Contact hrs** 60.0 h

Course offerings and teaching methods in academic year 2020-2021

A (semester 2)	Dutch	Gent	seminar: practical PC room classes	24.0 h
			project	24.0 h
			lecture	12.0 h

Lecturers in academic year 2020-2021

Van Cauwelaert, Dimitri	TW07	staff member
Veelaert, Peter	TW07	lecturer-in-charge

Offered in the following programmes in 2020-2021	**crdts**	**offering**
Bachelor of Science in Engineering Technology (main subject Electronics and ICT Engineering Technology)	6	A
Linking Course Master of Science in Electronics and ICT Engineering Technology (main subject Electronics Engineering)	6	A
Linking Course Master of Science in Electronics and ICT Engineering Technology (main subject Embedded Systems)	6	A
Linking Course Master of Science in Electronics and ICT Engineering Technology (main subject ICT)	6	A
Preparatory Course Master of Science in Electronics and ICT Engineering Technology (main subject Electronics Engineering)	6	A
Preparatory Course Master of Science in Electronics and ICT Engineering Technology (main subject Embedded Systems)	6	A
Preparatory Course Master of Science in Electronics and ICT Engineering Technology (main subject ICT)	6	A

Teaching languages

Dutch

Keywords

Hardware synthesis, VHDL

Position of the course

The overall objective is to acquire knowledge of VHDL, with emphasis on synthesis and simulation. Items that require particular attention are:

- the difference between software and hardware realizations of algorithms
- difference between models used for simulation and models used for synthesis
- generation of efficient hardware

Contents

Theory

- Digital design using hardware description languages
- Entities and architectures
- Signals and data types
- Dataflow description of combinational hardware
- Behavioural description of combinational hardware
- Event-driven simulation and test benches
- Modeling of sequential components (latches, flipflops, registers, counters)
- FSMs, ASM charts and RTL design in HDL

- Modeling busses and tri-state logic
- Packages, libraries, functions, procedures

Lab sessions
- Learning to use a toolchain
- HDL-descriptions using ASM charts
- Programming and testing models on FPGAs
- Time and performance analysis
- one more complex design task

Initial competences

To be familiar with digital components and the basics of digital design. Basic knowledge of VHDL.

Final competences

1 To design in a high-level description language (HDL)
2 To simulate a HDL design and to control the verification and validation process
3 To understand and use a complex toolchain
4 To design as a team

Conditions for credit contract

Access to this course unit via a credit contract is determined after successful competences assessment

Conditions for exam contract

This course unit cannot be taken via an exam contract

Teaching methods

Lecture, project, seminar: practical PC room classes

Extra information on the teaching methods

The lectures and the seminar are tightly connected. The theoretical concepts are first explained and immediately practised during lab sessions. After the basic competences have been acquired, they are applied in a larger project. Presence at all sessions is required.

Learning materials and price

Slides on Ufora.
Tasks, manual and VHDL study material on Ufora.

References

Kenneth Short, VHDL for Engineers
Sudhakar Yalamanchili, VHDL: From Simulation to Synthesis

Course content-related study coaching

Students are supervised intensively during contact hours. Students can ask questions during predefined hours or ask for further explanation or clarification by appointment. Additional guidance is provided through the electronic learning environment.

Evaluation methods

end-of-term evaluation

Examination methods in case of periodic evaluation during the first examination period

Oral examination, assignment

Examination methods in case of periodic evaluation during the second examination period

Oral examination, assignment

Examination methods in case of permanent evaluation

Job performance assessment, report

Possibilities of retake in case of permanent evaluation

examination during the second examination period is not possible

Extra information on the examination methods

Theoretical and practical knowledge are evaluated in an oral examination with written preparation.
The project evaluation is based on the report and oral presentation.

Calculation of the examination mark