VLSI Technology and Design (E031440)

Due to Covid 19, the education and evaluation methods may vary from the information displayed in the schedules and course details. Any changes will be communicated on Ufora.

Course Specifications
Valid as from the academic year 2019-2020

Course size

<table>
<thead>
<tr>
<th>Credits</th>
<th>Study time 180 h</th>
<th>Contact hrs</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.0</td>
<td></td>
<td>67.5 h</td>
</tr>
</tbody>
</table>

Course offerings and teaching methods in academic year 2020-2021

<table>
<thead>
<tr>
<th>Semester</th>
<th>Language</th>
<th>Mode</th>
<th>Project</th>
<th>Guided self-study</th>
</tr>
</thead>
<tbody>
<tr>
<td>A (1st)</td>
<td>English</td>
<td>project</td>
<td>30.0 h</td>
<td>30.0 h</td>
</tr>
<tr>
<td></td>
<td></td>
<td>lecture</td>
<td>30.0 h</td>
<td></td>
</tr>
<tr>
<td>B (1st)</td>
<td>Dutch</td>
<td>project</td>
<td>30.0 h</td>
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<tr>
<td></td>
<td></td>
<td>guided self-study</td>
<td>30.0 h</td>
<td></td>
</tr>
</tbody>
</table>

Lecturers in academic year 2020-2021

Doutreloigne, Jan
TW06 lecturer-in-charge

Offered in the following programmes in 2020-2021

<table>
<thead>
<tr>
<th>Programme</th>
<th>credits</th>
<th>offering</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bridging Programme Master of Science in Electrical</td>
<td>6</td>
<td>A</td>
</tr>
<tr>
<td>Engineering (main subject Electronic Circuits and</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Systems)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Master of Science in Electrical Engineering (main</td>
<td>6</td>
<td>A</td>
</tr>
<tr>
<td>subject Communication and Information Technology)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Master of Science in Electrical Engineering (main</td>
<td>6</td>
<td>A</td>
</tr>
<tr>
<td>subject Electronic Circuits and Systems)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Master of Science in Electrical Engineering</td>
<td>6</td>
<td>B</td>
</tr>
<tr>
<td>European Master of Science in Photonics</td>
<td>6</td>
<td>A</td>
</tr>
</tbody>
</table>

Teaching languages

Dutch, English

Keywords

VLSI, IC, CMOS, technology, design, simulation, PCB, layout

Position of the course

This course describes the basic technology and process flow for the fabrication of integrated CMOS circuits. Also the design (simulation on the basis of SPICE models and manual mask layout) of such CMOS ICs is extensively studied. Finally the course also pays attention to the interconnection of ICs by means of printed circuit boards (PCBs).

Contents

- VLSI technology: semiconductor physics, MOSFET, microelectronics and microsystems, process flow of an IC technology, packaging and assembly, multilayer PCB technology, virtual wafer fab
- VLSI design: SPICE modelling, CMOS IC design, parameter extraction, PCB design

Initial competences

- Basic knowledge of electronics

Final competences

1. Understand the process flow of modern IC technologies
2. Simulate and layout electronic circuits in modern IC technologies

Conditions for credit contract

Access to this course unit via a credit contract is determined after successful competences assessment

Conditions for exam contract

This course unit cannot be taken via an exam contract

(Approved)
Teaching methods
Guided self-study, lecture, project

Extra information on the teaching methods
Classroom lectures; Projects

Learning materials and price
Course notes can be downloaded from the electronic learning platform for free

References

Course content-related study coaching
Continuous guidance/support, for the theoretical classes as well as for the design project, during the whole semester by the responsible professor and a scientific coworker.

Evaluation methods
End-of-term evaluation and continuous assessment

Examination methods in case of periodic evaluation during the first examination period
Oral examination

Examination methods in case of periodic evaluation during the second examination period
Oral examination

Examination methods in case of permanent evaluation
Report

Possibilities of retake in case of permanent evaluation
Examination during the second examination period is possible in modified form

Extra information on the examination methods
During examination period: oral closed-book examination.
Outside examination period: report of the IC design project that takes about 1 month time (schematic design + simulations + layout).

Calculation of the examination mark
Evaluation during examination period: 70%
Evaluation outside examination period: 30%

(Approved)