GHENT UNIVERSITY

Course Specifications

Valid as from the academic year 2019-2020

Digital Electronics II (E731023)

Course size (nominal values; actual values may depend on programme)

Credits 6.0	Study time 180 h	Contact hrs	60.0 h

Course offerings and teaching methods in academic year 2019-2020

A (semester 1)	Dutch	practicum	24.0 h
		lecture	36.0 h
B (semester 1)		lecture	30.0 h

Lecturers in academic year 2019-2020

Veelaert, Peter	TW07	lecturer-in-charge

Offered in the following programmes in 2019-2020	crdts	offering
Bachelor of Science in Engineering Technology (main subject Electronics and ICT Engineering Technology)	6	A
Master of Science in Electrical Engineering Technology (main subject Automation)	6	A
Master of Science in Information Engineering Technology	3	B
Linking Course Master of Science in Electronics and ICT Engineering Technology (main subject Electronics Engineering)	6	A
Linking Course Master of Science in Electronics and ICT Engineering Technology (main subject ICT)	6	A
Preparatory Course Master of Science in Electronics and ICT Engineering Technology (main subject Electronics Engineering)	6	A
Preparatory Course Master of Science in Electronics and ICT Engineering Technology (main subject ICT)	6	A

Teaching languages

Dutch

Keywords

Digital Systems, VHDL, RTL-ontwerp, HDL

Position of the course

The course focuses on the design of complex digital circuits. The students are introduced to high-level description languages (VHDL) and the main methodology for the design of sequential circuits: register-transfer-level design. The emphasis is on generic design and the complexity and scalability of the circuits.

Contents

Course Offering A and B

1 Boolean expressions and logic gates. Two and multilevel circuits. Karnaugh maps and minimisation algorithms.
2 Hardware description languages. Introduction to VHDL
3 Common combinational components and their VHDL description: adders, binary multipliers, multiplexers, demultiplexers, encoders, decoders, switching networks, network trees.
4 Synchronous sequential logic: latches, flipflops, analysis of sequential circuits.
5 State reduction. Synthesis of sequential circuits and VHDL description of FSMs.
6 Common sequential circuits and their VDHL description: registers, shift registers, ripple counters, synchronous counters.
7 RTL-design. Datapath models. Algorithmic state machines (ASM). VHDL description of ASM.
8 Asynchronous design: races, cycles, hazards, state reduction, equivalence tables, merger graphs.

Course Offering B

1 Boolean expressions and logic gates. Two and multilevel circuits. Karnaugh maps and minimisation algorithms.
2 Hardware description languages. Introduction to VHDL
3 Common combinational components and their VHDL description: adders, binary multipliers, multiplexers, demultiplexers, encoders, decoders, switching networks, network trees.
4 Synchronous sequential logic: latches, flipflops, analysis of sequential circuits.
5 State reduction. Synthesis of sequential circuits and VHDL description of FSMs.
6 Common sequential circuits and their VDHL description: registers, shift registers, ripple counters, synchronous counters.
7 RTL-design. Datapath models. Algorithmic state machines (ASM). VHDL description of ASM.

Initial competences

Being familiar with the components and fundamentals of digital electronics: gates, multiplexers, latches, flipflops, finite state machines, Karnaugh maps. AD and DA conversion.

Final competences

1 **Course Offering A and B**
To analyze and design asynchronous circuits.
2 **Course Offering A and B**
To design at RTL level using ASM charts.
3 **Course Offering A and B**
To design digital circuits in VHDL.
4 **Course Offering A**
To understand the complexity and scalability of combinatorial and sequential circuits.

Conditions for credit contract

Access to this course unit via a credit contract is determined after successful competences assessment

Conditions for exam contract

This course unit cannot be taken via an exam contract

Teaching methods

Lecture, practicum

Learning materials and price

Syllabus for the theory, with handouts of slides. Laboratory assignments on the electronic learning environment, sometimes with solutions. Handouts for introduction to VHDL. Manuals for development boards. Reference sources VHDL.

References

Digital Design, 5th ed., Morris Mano and Michael Ciletti, Prentice-Hall, 2007

Course content-related study coaching

The lecturer is available during and after the lectures for further explanations. There is assistance during the lab sessions. Individual explanations are possible by appointment.

Evaluation methods

end-of-term evaluation and continuous assessment

Examination methods in case of periodic evaluation during the first examination period

Oral examination

Examination methods in case of periodic evaluation during the second examination period

Oral examination

Examination methods in case of permanent evaluation

Skills test, job performance assessment

Possibilities of retake in case of permanent evaluation

examination during the second examination period is not possible

Extra information on the examination methods

There is a closed-book exam for the theoretical part. The exam consists of four or five questions. For the lab sessions, there is a written test. In the second examination period it is only possible to resume the oral examination of the theoretical part.

Course Offering A and B
End-of-term evaluation and continuous assessment
Course Offering B
End-of-term evaluation

Calculation of the examination mark

Lab sessions: 1/3
Theoretical part: 2/3