GHENT UNIVERSITY

Course Specifications

Valid as from the academic year 2015-2016

Embedded Systems: Hardware Synthesis (E731029)

Course size (nominal values; actual values may depend on programme)

Credits 3.0	Study time 90 h	Contact hrs	36.0 h

Course offerings and teaching methods in academic year 2018-2019

A (semester 2)	Dutch	project	12.0 h
		practicum	24.0 h

Lecturers in academic year 2018-2019

Veelaert, Peter	TW07	lecturer-in-charge

Offered in the following programmes in 2018-2019	crdts	offering
Bachelor of Science in Engineering Technology (main subject Electronics and ICT Engineering Technology)	3	A
Bachelor of Science in Electronics and ICT Engineering Technology	3	A
Linking Course Master of Science in Electronics and ICT Engineering Technology (main subject Electronics Engineering)	3	A
Linking Course Master of Science in Electronics and ICT Engineering Technology (main subject ICT)	3	A
Preparatory Course Master of Science in Electronics and ICT Engineering Technology (main subject Electronics Engineering)	3	A
Preparatory Course Master of Science in Electronics and ICT Engineering Technology (main subject ICT)	3	A

Teaching languages

Dutch

Keywords

VHDL, Digital electronics design

Position of the course

The overall objective is to acquire knowledge on VHDL, with emphasis on synthesis and simulation. Items that require particular attention are:

- the difference between software and hardware realizations of algorithms
- difference between models used for simulation and models used for synthesis
- inference of efficient hardware

Contents

Theoretical part

1 Introduction to generic digital design
2 Introduction to simulation and synthesis
3 VHDL as hardware description language
4 Structural and dataflow descriptions
5 Modeling combinational components
6 Modeling memory components
7 Verification

Lab exercises

- learning a toolchain
- VHDL descriptions with ASM charts
- Programming and testing models in CPLD and FPGA
- Time and performance analysis

Initial competences

To be familiar with digital components and the basics of digital design

Final competences

1 To design in a high-level description language (HDL)
2 To simulate a HDL design and to control the verification and validation process
3 To understand and use a complex toolchain
4 To understand the difference between hardware and software descriptions

Conditions for credit contract

Access to this course unit via a credit contract is determined after successful competences assessment

Conditions for exam contract

This course unit cannot be taken via an exam contract

Teaching methods

Guided self-study, practicum, project

Extra information on the teaching methods

The labsessions and guided self study are tightly connected. The theoretical concepts are explained, and immediatley practised during lab sessions. There is also a project. Presence at all sessions is required. The contact hours are distributed as follows:
- lab sessions and guided self study: 24
- project sessions: 12

Learning materials and price

Hardware description and simulation in VHDL, Steven Redant
Slides on Minerva
Tasks, tutorials and VHDL background material on Minerva

References

VHDL, A Starters Guide, Sudhakar Yalamanchili
Introductory VHDL from Simulation to Synthesis, Sudhakar Yalamanchili

Course content-related study coaching

Students are supervised intensively during contact hours. Students can ask questions during predefined hours or ask for further explanation or clarification by appointment. Additional guidance is provided through the electronic learning environment.

Evaluation methods

end-of-term evaluation

Examination methods in case of periodic evaluation during the first examination period

Oral examination, assignment

Examination methods in case of periodic evaluation during the second examination period

Oral examination, assignment

Examination methods in case of permanent evaluation

Possibilities of retake in case of permanent evaluation

examination during the second examination period is not possible

Extra information on the examination methods

The lab sessions and the self study are assessed in an oral exam with written preparation.
The project will be assessed on the basis of the report and an oral presentation.

Calculation of the examination mark

Project: 2/3
Self study and lab sessions: 1/3