GHENT UNIVERSITY

Course Specifications

Valid as from the academic year 2016-2017

Digital Building Blocks (E031341)

Course size (nominal values; actual values may depend on programme)

Credits	6.0	Study time	180 h
Contact hrs	52.5 h		

Course offerings and teaching methods in academic year 2018-2019

A (semester 2)	Dutch	self-reliant study activities	10.0 h
		lecture	35.0 h
		practicum	20.0 h

Lecturers in academic year 2018-2019

Doutreloigne, Jan	TW06	lecturer-in-charge

Offered in the following programmes in 2018-2019	crdts	offering
Master of Science in Electrical Engineering (main subject Communication and Information Technology)	6	A
Master of Science in Electrical Engineering (main subject Electronic Circuits and Systems)	6	A
Master of Science in Computer Science Engineering	6	A
Master of Science in Computer Science Engineering	6	A
Master of Science in Electrical Engineering	6	A

Teaching languages

Dutch

Keywords

digital CMOS circuits, power dissipation, speed, deep-submicron, micro-electronics

Position of the course

This course aims at acquiring knowledge and expertise in the design of good digital CMOS circuits that can be used as building blocks in digital system design.
The circuits are studied at circuit level and logic level, and important metrics like area, speed and dissipation are addressed. The lab work involves the effective design of circuits and the analysis of their properties using modern CAD software. To get acquainted with scientific literature, an advanced digital circuit design topic is studied in small groups and the results are presented to the class.

Contents

- Introduction: metrics for digital circuits
- CMOS Semiconductor components: semiconductor properties, the CMOS diode, the MOSFET transistor
- Post-CMOS technologies
- Integrated wires: properties, design
- Combinational CMOS Circuits: the CMOS Inverter, static circuits, dynamic circuits
- Sequential CMOS Circuits: static circuits, dynamic circuits
- Timing and Clock Distribution: timing and synchronisation of sequential circuits, synchronous circuits
- Special Building Blocks: arithmetic building blocks, memories
- Standard-cell design flow: optimization, technology mapping, automated physical design (placement, routing)
- Testing and testability
- Design, layout and characterize simple digital building blocks (logic gates, flipflops)
- Advanced topics in research and development: topics depending on recent evolutions and class preferences

Initial competences

Required prior knowledge: linear electrical networks (charge, current, potential, voltage, power, resistance, capacitance, induction, rc-networks), basic knowledge about digital gates (AND, OR, INVERTOR, ...), elementary logic synthesis, , combinational and sequential digital circuits, basic knowledge of computer architecture (components of a processor, memory hierarchy, ALU-components: binary addition, multiplication, ...), switch model for the MOSFET transistor, physical meaning of the term 'semiconductor', notions of VLSI-technology (physical structure of a MOSFET, most common process steps)

At Ghent University, this can be obtained by following:
- the Bachelor electrical engineering courses: Electrical networks, Digital electronics, Computer architecture;
- or the Bachelor informatics courses: Introductory electronics, Computer architecture;

Final competences

1 Thouroughly understand the operation of nanoscale MOSFET transistors.
2 Understand the impact of scaling on the properties of integrated digital gates and interconnections.
3 Know the structure and properties of the most common families of digital gates and memory cells.
4 Understand the principles of fundamental approaches to technology-dependent optimization at the logic level and apply these techniques to simple examples.
5 Explain the principles and main difficulties of technology mapping, placement, routing and testing.
6 Design digital gates at the transistor level, from schematic design to lay-out, including the back-annotation of lay-out information to performance analysis.

Conditions for credit contract

Access to this course unit via a credit contract is determined after successful competences assessment

Conditions for exam contract

This course unit cannot be taken via an exam contract

Teaching methods

Lecture, practicum, self-reliant study activities

Learning materials and price

Presentation material (dutch); textbook J. Rabaey, A. Chandrakasan, B. Nikolic: "Digital Integrated Circuits", Prentice-Hall, New Jersey, 2003. ISBN 0-13-120764-4 (textbook is mandatory for non Dutch speaking students)

References

- J. Rabaey, A. Chandrakasan, B. Nikolic: "Digital Integrated Circuits", Prentice-Hall, New Jersey, 2003. ISBN 0-13-120764-4
- L. Solymar, D. Walsh: "Electrical properties of materials", seventh edition, Oxford University Press, Oxford, UK, 2004. ISBN 0-19-926793-6
- D. Gizopoulos (Ed.): "Advances in Electronic Testing: Challenges and Methodologies", Springer, Frontiers in Electronic Testing, 2006. ISBN 0-387-29408-2

Course content-related study coaching

Coaching of lab sessions and literature study; thematic online discussion forums for questions; individual coaching on request before or after classes or by appointment.

Evaluation methods

end-of-term evaluation and continuous assessment

Examination methods in case of periodic evaluation during the first examination period

Oral examination

Examination methods in case of periodic evaluation during the second examination period

Oral examination

Examination methods in case of permanent evaluation

Participation, assignment, skills test, peer assessment, report

Possibilities of retake in case of permanent evaluation

examination during the second examination period is not possible

Extra information on the examination methods

During examination period: oral closed-book exam, written preparation with open

book.
During semester: graded lab sessions and lab reports; graded project (including peer-evaluation).
Frequency: 3 lab exercises of multiple sessions each with written report + a study project with presentation.

Calculation of the examination mark

Special conditions: Lab work (including project) and exam each account for 50% of total score, but in order to succeed, a score of at least 9/20 must be attained on each part; scores below 9/20 on either part can not be compensated. Project and lab work do not count for second session: there is only a single exam to evaluate whether the required competences have been attained (if you failed for the evaluation during the semester, an alternative assignment will be part of this exam).